WHAT IS CLAIMED IS:

1. A data encoding/decoding apparatus comprising:

a decoder decoding a coded stream, which is formed in a first format and inputted on real time, to generate video data and audio data;

a video output memory storing the video data from the decoder;

an audio output memory storing the audio data from the decoder;

a video input memory provided to be connected to the decoder through a first data path when the coded stream of the first format is transcoded to generate a second stream formed in a second format;

an audio input memory provided to be connected to the decoder through a second data path when the transcoding is performed; and

an encoder encoding the video data from the video input memory and the audio data from the audio input memory to generate the second stream of the second format.

2. The data encoding/decoding apparatus of claim 1 wherein, when the transcoding is performed, the first data path and the second data path are set from OFF state to ON state, so that the video data output from the decoder is stored in the video input memory through the first data path and the audio data output from the decoder is stored in the audio input memory through the second data path.

3. The data encoding/decoding apparatus of claim 1 further comprising:

a video output interface outputting the video data stored in the video output memory to an external device in a predetermined format at predetermined times; and

an audio output interface outputting the audio data stored in the audio output memory to an exterior device in a predetermined format at predetermined times.

4. The data encoding/decoding apparatus of claim 1 further comprising:

a video input interface storing in the video input memory video data which is inputted from an external device at predetermined times; and

an audio input interface storing in the audio input memory audio data which is inputted from an external device at predetermined times.

5. The data encoding/decoding apparatus of claim 1 further comprising a clock generating unit generating a clock signal for circuit components of the data encoding/decoding apparatus wherein the clock signal from the clock generating unit is supplies to each circuit component without adjusting a phase of the clock signal based on clock reference information of the coded stream inputted on real time.

6. A decoding apparatus for use with an external encoder connected to the decoding apparatus, comprising:

a decoder decoding a coded stream, which is formed in a first format and inputted on real time, to generate video data and audio data;

a video output memory storing the video data from the decoder;

an audio output memory storing the audio data from the decoder;

a first data path provided to deliver the video data from the decoder to the external encoder, the first data path connecting the decoder and the external encoder when the coded stream of the first format is transcoded to generate a second stream formed in a second format; and

a second data path provided to deliver the audio data from the decoder to the external encoder when the transcoding is performed.

7. The decoding apparatus of claim 6 wherein, when the transcoding is performed, the first data path and the second data path are set from OFF state to ON state, so that the video data output from the decoder is delivered to the external encoder through the first data path and the audio data output from the decoder is delivered to the external encoder through the second data path.

8. The data encoding/decoding apparatus of claim 1 wherein the coded stream of the first format is at least one of a MPEG2 transport stream and a digital video stream.

9. The data encoding/decoding apparatus of claim 1 wherein the second stream of the second format is at least one of a MPEG2 program stream and a MPEG4 program stream.

10. The decoding apparatus of claim 6 further comprising a clock generating unit generating a clock signal for circuit components of the decoding apparatus wherein the clock signal from the clock generating unit is supplies to each circuit component without adjusting a phase of the clock signal based on clock reference information of the coded stream inputted on real time.